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RESEARCH

The artificially intelligent switching framework for terminal access provides smart routing in modern computer networks

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The main page of the web interface provides access to various switch settings and displays all the necessary information about the device. Admins can quickly view device status, performance statistics, etc., as well as make necessary settings. The switch's command-line interface is accessed by connecting a terminal or personal computer with a terminal emulation program installed on the switch's console port. In this paper, the intelligent switching framework was introduced for terminal access to provide smart routing. This access method is most useful when connecting to the switch first when the Internet protocol (IP) address is unknown or not set, when password recovery is required, or when performing advanced switch settings. The command line interface can also be accessed over the network using the Telnet protocol. The user can use any administrative interface convenient to him to configure the switch because the set of functions available through the different management interfaces is the same for each.

Keywords: framework, routing, switching, command, interface, terminal access

Introduction

It also worth mentioning the possibility of updating the software of the switches (except for unmanaged ones) (1). This ensures a long service life of the devices as new versions of the software are released, allowing you to add new features or remove existing bugs, which greatly simplifies and reduces the cost of using the devices (2). D-Link distributes new versions of software free of charge.

You can also add the ability to save switch settings in case of subsequent reconfiguration or replication failures, saving the administrator from doing routine work. A large number of command line interface (CLI) commands are available (3). Commands are complex, multilevel, require a large number of input parameters, or are simple and have a single parameter (4).

When working in the CLI, you can enter an abbreviated version of the command (5). For example, if you enter the command "show," the switch interprets this command as "show switch." Show commands are a convenient means of checking switch status and parameters and providing information needed to monitor and troubleshoot switch operation (6).

Another way to manage the switch is to use the simple network management protocol (SNMP) protocol. D-Link switches support SNMP versions 1, 2c, and 3. Most modern switches support various management and monitoring functions (7). It includes a user-friendly web-based management interface, CLI, Telnet, and SNMP management (8).

T-Link Smart Series switches support initial configuration and software updates through the T-Link Smart Console Utility. A web-based management interface allows you to configure and monitor switch settings using any computer

with a standard web browser (9). The browser is a universal access tool and can connect directly to the switch via hypertext transfer protocol.

The main web interface provides access to various switch settings and displays all the necessary information about the device (10). Admins can quickly view device status, performance statistics, etc., as well as make necessary settings (11).

The switch's CLI is accessed by connecting a terminal or personal computer with terminal emulation installed to the switch's console port (12). This access method is most useful when connecting to the switch first when the IP address is unknown or not set, when password recovery is required, or when performing advanced switch settings (13). The CLI can also be accessed over the network using the Telnet protocol.

The user can use any administrative interface convenient to him to configure the switch (14). The set of functions available through the different control interfaces is the same for each specific model. Another way to manage the switch is to use SNMP (15).

Simple network management protocol is a Layer 7 protocol of the OSI model that is specifically designed for managing and monitoring network devices and communications applications (16). This is done by exchanging control information between agents on network devices and managers located at control stations. D-Link switches support SNMP versions 1, 2c, and 3 (17).

It is also worth mentioning the possibility of updating the software of the switches (except for unmanaged ones). This ensures a long service life of the devices and allows you to add new features or remove existing bugs when new versions of the software are released, which greatly simplifies and reduces the cost of using the devices (18). D-Link distributes new software versions free of charge. It can also add the ability to save switch settings in case of subsequent reconfiguration or replication failures, saving the administrator from doing routine work (19).

Literature review

In operating mode, the local and system memory for the video card are logically equal. Configurations are never stored in the local storage system memory. Therefore, relatively small, randomly located fragments must be selected from memory (20).

As system memory is dynamic in 4K blocks in this mode, it is necessary to provide a mechanism to map serial addresses to actual addresses of 4-kilobyte blocks in system memory to ensure acceptable performance. In this case, addresses that never lie within the GART variety are not changed and are mapped directly to system memory or device-specific range memory (21).

To generate a sequence of requests without waiting for the current operation to complete, this also increases bus speed. As a result of the new low-voltage power specifications, four transactions (data block transfers) can be carried out in one 66 MHz cycle [accelerated graphics port (AGP) 4x], which means 1 GB/s bus throughput (22). The only thing that is not completely happy is that the device can dynamically switch between all the required modes; this is not necessary for anyone (23).

However, video processing needs and demands are increasing, and Intel is preparing a new specification aimed at meeting the needs of high-performance graphics workstations (24). The main direction is to increase the power supply of graphic cards. For this, new electrical connections have been added to the AGP Pro connector.

Accelerated graphics port Pro cards are supposed to be of two types: high- and low-power (25). The video cards with an AGP version 3.0 interface (often referred to as AGP 8x) went into mass production. A 2-fold increase in performance was achieved by increasing the bus clock frequency to 66 MHz and using a new signal level of 0.8 V (AGP 2.0 used the 1.5 V level). Therefore, while maintaining the basic parameters of the interface, it was possible to increase the bus performance to approximately 2132 MB/s (26).

Proposed model

Before you begin configuring the switch, you must establish a physical connection between it and the workstation. Two types of cabling are used to manage the switch. The first type is through the console port (if the device has one), and the second type is through the Ethernet port (using the Telnet protocol or via a web interface).

The console port is used for initial switch configuration and typically requires no configuration. To access the switch through its Ethernet port, you must enter the default IP address of its management interface into a browser (usually listed in the user manual). These slots can be used by the card as additional mounts, additional power supplies, or even transfer data via the peripheral component interconnect (PCI) bus! At the same time, only minor restrictions are imposed on the use of these spaces.

- Never use the V I/O lines to power them.
- Do not set the M66EN line (pin 49 V) to GND (this is quite normal as it puts the PCI bus in 33 MHz mode).

When using a bus transfer slot:

- The PCI I/O subsystem must be designed for 3.3 V and capable of operating at 5 V.
- The specification requires a free PCI slot to provide cooling.

When connecting to a copper (RJ-45 connector) Ethernet switch port on Ethernet-compatible servers, routers, or workstations, use a four-pair Type 5, 5e, or 6 UTP cable

for Gigabit Ethernet. D-Link switches support auto-polarity detection (MDI/MDIX), so any type of cable (straight or crossover) can be used. At the same time, all AGP Pro retail cards should have a special overlay with a width of 3 or 2 slots, respectively, while the card acquires an intimidating appearance.

- Show configuration: used to display the currently created or saved configuration in NVRAM,
- Show fdb: used to show the current switch table,
- Show swtch: used to display general information about a switch,
- Show device_state: used to display internal and external power status,
- Show error ports: used to display error statistics for a given range of ports,
- Show packet ports: used to display statistics about packets sent and received by a port,
- Show firmware information: used to display information about the switching software (firmware),
- Show ipif: used to display information about the IP interface settings on the switch, and
- Show log: switch is used to view the log file.

If the switch ports support automatic polarity detection, you can use any 4-pair Type 5, 5e, or 6 UTP cable to connect to the copper (RJ-45 connector) Ethernet port. Otherwise, a crossover cable should be used. The LED indication of the correct connection port will help to determine.

If the corresponding indicator lights up, the connection between the switch and the connected device is established. If the indicator is off, one of the devices may not be powered on, there may be a problem with the connected device's LAN adapter, or there may be a cable problem. If the indicator turns on and off, there may be problems with automatic speed detection and operation mode. This was shown in **Figure 1**.

- Unmanaged switches: These switches do not support management capabilities and software updates.

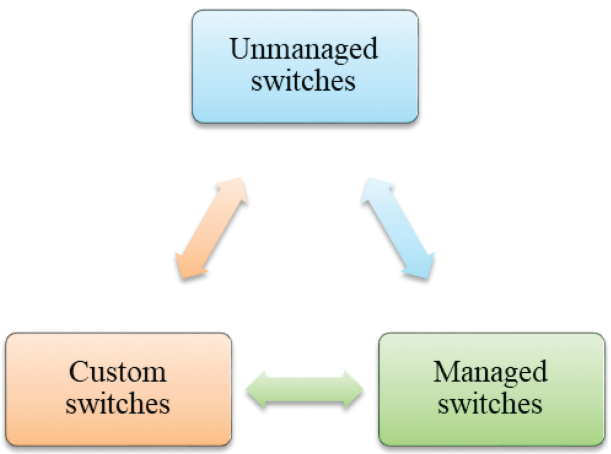

FIGURE 1 | Different types of switches.

- Managed switches: These switches are complex devices that allow you to perform extended functions of layers 2 and 3 of the OSI model. Switches can be managed through web interface, CLI, SNMP protocol, Telnet, etc.
- Custom switches: These switches occupy an intermediate position between them. They offer users the ability to configure certain network settings using intuitive management applications, a web interface, a simple CLI, and the SNMP protocol.

In DMA mode, the main memory is the memory on the card. The setting is stored in memory but is copied to the graphics card's local memory before use. Thus, the AGP interface acts as a "cartridge carrier" (system) to the "firing position" (local memory).

The transmission is carried out in large sequential data packets. Version AGP 2.0 provides for the implementation of four transactions (data block transfers) per cycle (AGP 4x method, quadruple multiplication) due to the use of low-voltage power specifications. Although the connector is mechanically compatible with AGP 2.0, its electrical characteristics have changed due to the voltage drop on the signal lines. The AGP bus is now being replaced by the PCI Express serial bus on modern platforms.

D-Link-managed switches are equipped with a console port. Depending on the switch model, the console port may have a DB-9 or RJ-45 connector. The switch is connected to the computer's serial port using the console cable included in the package.

A console connection is sometimes referred to as an "out-of-band connection." This means the console uses a different network connection scheme (not using the bandwidth of the Ethernet ports). After connecting the switch console port to a personal computer, you need to run a VT100 terminal emulation program (such as the HyperTerminal program in Windows).

The program should set the following connection parameters, which are usually specified in the documentation for the device: As is always the case in the computer industry, the problem is not solved. Here's what seems like a simple solution for you: switch to a 66 MHz, 64-bit PCI bus with a larger bandwidth, but no. Based on the same PCI R2.1 standard, Intel creates a new bus, AGP (R1.0, then 2.0), which differs from its "parent" in the following ways, as shown in **Figure 2**:

- Transmitting mode.
- Multiplexing mode.
- Pipelining mode.
- Storage mode.

The irony is that video cards still want to have more memory, but no one saves settings in computer memory because there are practically no structures for such a

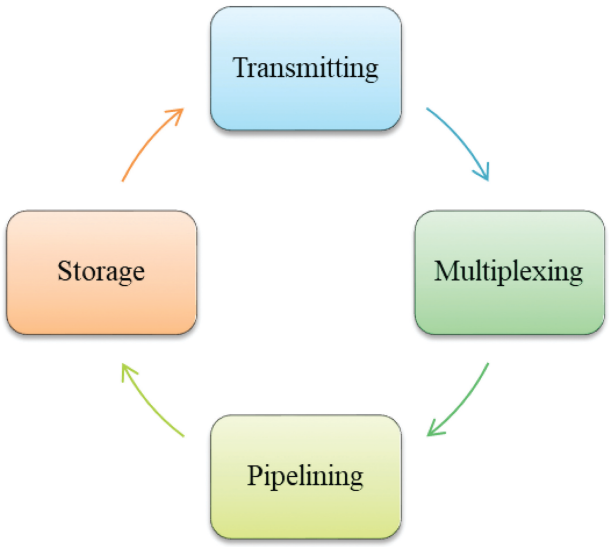

FIGURE 2 | Proposed system design.

module (yet, I emphasize). At the same time, as the cost of memory in general drops, cards don't particularly rise in price. However, almost everyone believes that AGP has a bright future, and that the rapid growth of multimedia applications (particularly games) will soon render the system unsuitable for memory.

So, without going into particularly technical details, it makes sense to explain how it all works. Therefore, AGP acts as a "back-end system," providing timely "delivery of cartridges" (fluxes) to the front-end (in local memory). Transmission is carried out in large, contiguous packets.

Results and discussion

The proposed intelligent switching framework (ISF) was compared with the existing fast computational networking framework (FCNF), zero trust architecture (ZTA), heterogeneous data exchange platform (HDEP), and QoS localized routing scheme (QLRS).

Transfer mode management

This realization that a further increase in the overall performance of a personal computer "rests" in the video subsystem led to the proposal to allocate a separate accelerated graphics port (AGP) interface bus to send one stream of video data at a time. This standard quickly replaced the previous interfaces used by video cards, including ISA, VLB, and PCI. The comparison of transfer mode management is shown in **Table 1**.

The comparison of transfer mode management is shown in **Figure 3**. The main advantage of AGP bus is their high efficiency. If the ISA bus allows transfers up to 5.5 MB/s, VLB allows transfers up to 130 MB/s, and PCI allows transfers up to 133 MB/s, the AGP bus theoretically has a peak bandwidth of up to 1066 MB/s (in the transfer mode of four 32-bit words).

TABLE 1 | Comparison of transfer mode management.

Data	FCNF	ZTA	HDEP	QLRS	ISF
100	43.98	44.73	55.08	80.15	84.90
200	44.32	46.14	55.82	81.02	86.45
300	44.66	47.55	56.56	81.89	88.00
400	45.00	48.96	57.30	82.76	89.55
500	45.34	50.37	58.04	83.63	91.10
600	45.68	51.78	58.78	84.50	92.65
700	46.02	53.19	59.52	85.37	94.20

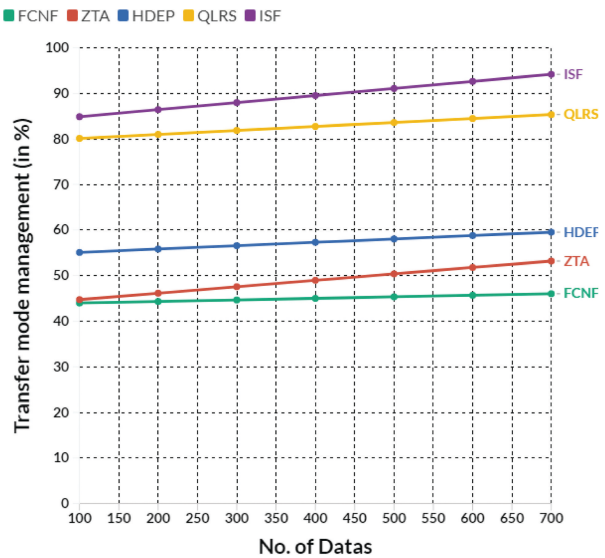

FIGURE 3 | Comparison of transfer mode management.

Buffer management

Intel developed the AGP interface to solve two major problems associated with processing three-dimensional (3D) graphics on a personal computer. First, the 3D graphics system must allocate as much memory as possible to store the data and z-buffer. The more texture maps available for 3D applications, the better the image will look on the monitor screen. The comparison of buffer management is shown in **Table 2**.

Figure 4 depicts a buffer management comparison. In general, the same memory is used for settings as for the Z-buffer. Video controller developers could use conventional random access memory (RAM) to store texture and z-buffer information, but the bandwidth of the PCI bus was a severe limitation here.

Bus management

The AGP bus connects the graphics subsystem to the system memory management unit, sharing access with the system's central processing unit (CPU). With AGP, only one type of device can be connected— graphics cards. At the same time, video controllers are built into the motherboard and cannot be upgraded using the AGP interface. The comparison of bus management is shown in Table 3.

Figure 5 shows the comparison of bus management. For an AGP controller, the specific physical address where information is stored in RAM is not important. This is the main solution of the new technology, which provides access to graphic data as a single block, regardless of the physical "scattering" of information across memory blocks. Additionally, the AGP operates with a system bus frequency of up to 133 MHz.

TABLE 2 | Comparison of buffer management.

Data	FCNF	ZTA	HDEP	QLRS	ISF
100	50.30	51.50	60.51	85.63	91.67
200	51.57	52.58	61.52	86.49	92.86
300	52.83	53.65	62.53	87.36	94.04
400	54.10	54.73	63.54	88.22	95.23
500	55.36	55.80	64.55	89.09	96.41
600	56.63	56.88	65.56	89.95	97.60
700	57.89	57.95	66.57	90.82	98.78

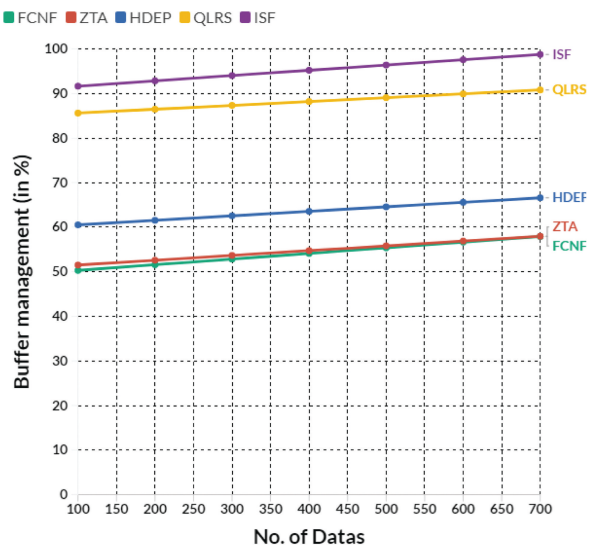

FIGURE 4 | Comparison of buffer management.

PCI management

The AGP specification is actually based on the PCI version 2.1 standard, but differs from it in key ways, like the fact that the bus is capable of transmitting two (AGP 2x), four (AGP 4x), or eight (AGP 8x) data blocks per cycle. The multiplexing of address and data lines is eliminated, and the pipeline of read/write operations eliminates the impact of latency in memory blocks on the speed of operations. The comparison of PCI management is shown in Table 4.

Figure 6 shows the comparison of PCI management. The PCI bandwidth was too small for real-time graphics processing. Intel solved this problem by introducing the AGP bus standard. Second, the AGP interface provides a direct connection between the graphics subsystem and RAM.

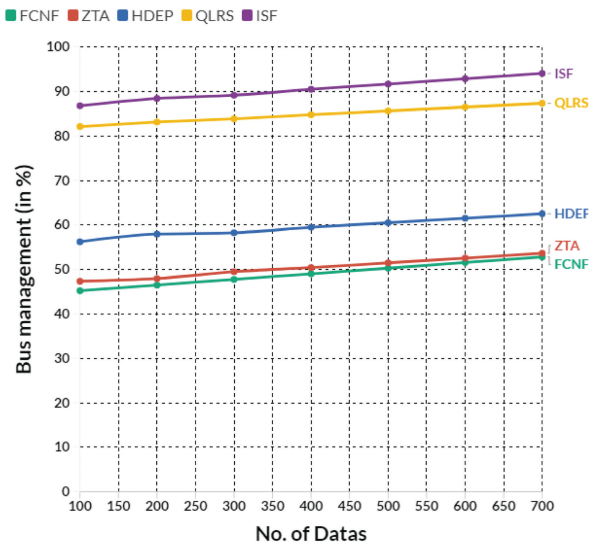

FIGURE 5 | Comparison of bus management.

TABLE 3 | Comparison of bus management.

Data	FCNF	ZTA	HDEP	QLRS	ISF
100	45.24	47.36	56.23	82.12	86.78
200	46.51	47.96	57.95	83.12	88.42
300	47.77	49.51	58.25	83.85	89.15
400	49.04	50.43	59.50	84.76	90.49
500	50.30	51.50	60.51	85.62	91.67
600	51.57	52.58	61.52	86.49	92.86
700	52.84	53.66	62.53	87.35	94.05

TABLE 4 | Comparison of PCI management.

Data	FCNF	ZTA	HDEP	QLRS	ISF
100	33.86	51.67	53.26	74.75	89.39
200	33.94	51.58	53.06	74.88	89.43
300	33.93	51.45	52.80	74.90	89.46
400	33.58	51.03	52.17	74.47	89.48
500	35.29	53.34	59.12	79.61	89.52
600	35.81	53.70	61.43	81.13	89.61
700	36.33	54.06	63.74	82.65	89.69

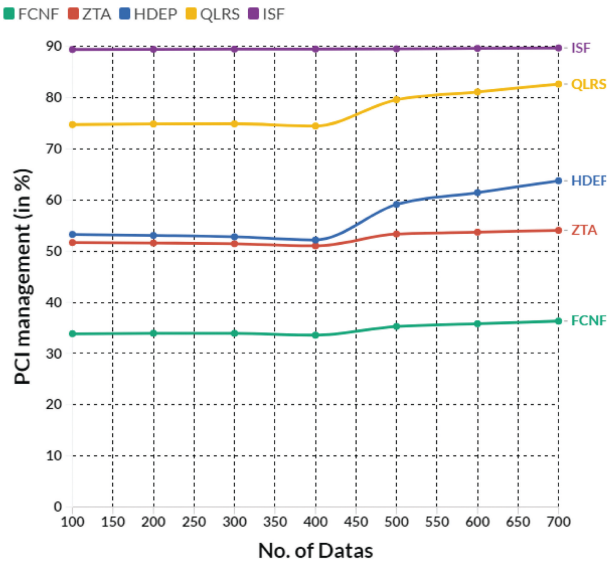

FIGURE 6 | Comparison of PCI management.

Therefore, the requirements of real-time 3D graphics output are met, and frame buffer memory is used more efficiently, thereby increasing 2D graphics processing speed.

Conclusion

Initially, video cards were built according to the following principles: Everything written by the central processor to the video memory is converted into an analog video signal, which is presented to the monitor according to strictly defined instructions. Therefore, the central processor must calculate the parameters of all the points to be displayed on the screen at this time and load all the data into the video memory.

Any change on the screen, even if it is a mouse trace, is the result of the work of the central processor. Accordingly, the higher the resolution and the number of colors used, the more time the processor spends calculating all the points of the created raster. Since the personal computer has become inextricably linked with the Windows graphical interface and various three-dimensional games over time, hardware developers have taken many steps to improve the standard video card in order to save the central processor from unnecessary work in initial drawing. Such devices are called "graphics accelerators."

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